

# A Highly Linear Bipolar 1V Folded Cascode 1.9GHz Low Noise Amplifier

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## Abstract

We present a 1V 1.9GHz cascode bipolar LNA, which dissipates 4mW, has a gain of 10.9dB, NF of 2.3dB, and an  $IP_3$  of -3.7dB. The relatively high linearity was achieved without compromising power dissipation, gain, and noise figure in comparison to a conventional cascode LNA.

## I. Introduction

The demand for low voltage and low power in RF transceivers has motivated designers to develop new circuit topologies to optimize noise, power dissipation, and linearity. While low voltage low noise amplifiers (LNA) have been designed between 1 to 2 Volts [1-3], the key factor that constrains the low voltage/power RF design is the limited options in topology. We present a low voltage LNA that has been realized in a RF IC bipolar process. This topology is best described as a folded cascode structure. The topology uses capacitively coupled LC resonating elements to reduce the voltage supply, but still maintain a relatively high linearity without sacrificing either noise figure or gain.

## II. Circuit Topology

Many of the circuit topologies used in RFIC functional blocks (e.g. LNA's and mixers) use DC current sharing to realize the necessary biasing, functionality, and also the performance. Figure 1a shows an example of a conventional cascode RF amplifier. This topology requires two stacked transistors for functionality

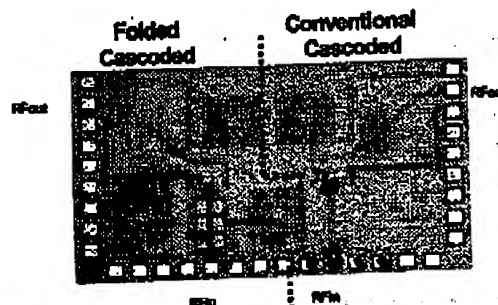


Figure 2: Chip micrograph showing the 1.9GHz folded cascode and conventional cascode low noise amplifiers.

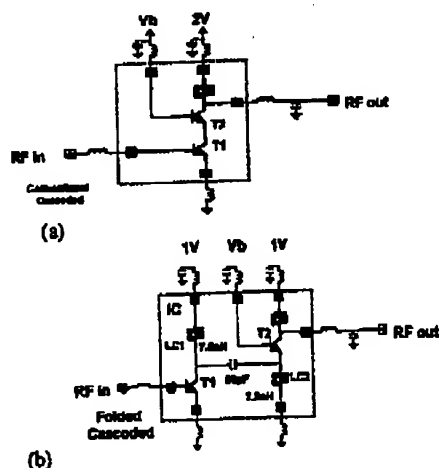


Figure 1: (a) 2V conventional cascode (b) 1V low voltage folded cascode with RF traps represented by on chip inductors. Both structures can be matched for input power and noise.

The conventional cascode offers higher stability and allows simultaneous matching for both noise and impedance [4]. If each transistor has a turn on voltage of 0.8V (i.e. the turn on voltage of a BJT), the absolute minimum supply voltage required is 1.6V. For the conventional cascode amplifier, both DC and AC currents are shared between the two transistors. If one could decouple the AC and DC currents the DC voltage supply could be reduced. Figure 1b depicts the proposed decoupling scheme. In this topology two on chip "RF traps", consisting of 7.5nH inductors are connected via a coupling capacitor in an anti-symmetric  $\pi$ -type network.

This "anti-symmetry" originates from the fact that the RF trap (LC1) is connected between the collector of transistor T1 and the DC supply, whereas the RF trap (LC2) is connected between the emitter of T2 and the RF/DC ground. The inductor connected to the collector of T2 functions as a relatively high impedance load at RF; the term "relatively high" shall be clarified through design. However, the RF traps provide a low DC impedance. The

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coupling capacitor couples the RF signal between transistors T1 and T2. This arrangement ensures that there is no DC current sharing between the two transistors. Furthermore, since the RF traps require no additional DC headroom, the required minimum voltage supply is only 0.8V, instead of 1.6V. The inductors that make up the RF traps could consist of either on chip spiral inductors or bond-wires. In our design, both on chip spiral inductors and bond-wires were used.

### III. Analysis and Design

For the circuit to operate as a cascode, the following conditions need to be enforced (i) The bulk of the RF collector current generated by T1 (i.e.  $g_{m1}v_{in}$ ) should be fed into the transconductance  $g_{m2}$  of T2. (ii) The gain at the equivalent output node of T1, relative to the input voltage ( $v_{in}$ ) should be near unity (this is to reduce the overall Miller effect). At RF, in order for the input current from T1 (i.e.  $g_{m1}v_{in}$ ) to drive the output resistance (i.e.  $1/g_{m2}$ ) of T2, one requires the LC tanks to have a relatively high impedance. Since the Q's of on chip inductors are finite in value, the resistance of the LC network is also finite in value at resonance. The equivalent resistance at resonance of the LC tanks is given by,

$$R_{e1} = R_1(1+Q_1^2) \quad (1)$$

$$R_{e2} = R_2(1+Q_2^2) \quad (2)$$

where  $R_1$  and  $R_2$  represent the series resistance of the inductors  $L_1$  and  $L_2$  at RF, respectively, and  $R_{e1}$  and  $R_{e2}$  denote the resistance of the LC<sub>1</sub> and LC<sub>2</sub> tanks at resonance, respectively. The key in designing these RF traps is to control the RF coupling between the RF traps and the transistor elements, T1 and T2 through the coupling capacitor. For the proper functionality of the circuit, the RF traps should have a high impedance in comparison to the impedance seen at the emitter of T2. This condition is enforced if,

$$R_{e1} \gg \left| \frac{1}{j\omega_0 C_{12}} + \frac{R_{e2}}{1+g_{m2}R_{e2}} \right| \quad (3)$$

and,

$$R_{e2} \gg \frac{1}{g_{m2}} \quad (4)$$

By using typical values for the design components one can check to see if conditions (3) and (4) are reasonable. The effective impedance at 1.9GHz for an on chip 7.5nH inductor with Q-factor of 5 (excluding the external bond wires) is  $\sim 90\Omega$ . Likewise, a coupling capacitance of value  $C_{12} \sim 60\text{pF}$  has an effective impedance of  $1.4\Omega$ . At a RF frequency of 1.9GHz and a Q of 5,  $R_{e1} = R_{e2} = 500\Omega$ . Equation (3) thus predicts that  $1/g_{m2} \ll 500\Omega$ . Hence for a collector current of 2mA, the transconductance for the

second stage is approximately  $1/g_{m2} \sim 13\Omega$ . Therefore conditions (3) and (4) can be easily satisfied.

To compare the functionality and performance of the low voltage folded cascode topology at 1V, a comparison was made with a conventional cascode amplifier at 1.9GHz operating at 2V fabricated on the same chip.

A mature 25GHz RF bipolar process was used to fabricate the circuits. The technology is described in [4]. Chip layout is shown in Figure 2. Figure 2 illustrates the chip layout for both topologies (i.e. the folded cascode and the classic cascode). Both circuits were simulated using HSPICE and Libra. The on-chip inductors were simulated using models extracted from measurement results.

The details of the design are provided below:

#### DC Biasing

The transistors were biased such that the unity current gain cut off frequency,  $f_t$  was approximately five times the RF operating frequency of 1.9GHz. To achieve this, a total collector current of 4mA (i.e. 2mA per transistor) was required for properly biasing the low voltage structure. The collector-emitter and the base-emitter voltages for this structure were set to 1V and 0.81V, respectively. The conventional cascode was biased at 2V with a total collector current of 2 mA. The collector-base voltage of T2 for the structure was set to 1.81 V.

#### Power Matching Circuit

The input and output ports of the LNA's were power matched with off chip moderately high Q lumped LC components on a 0.063-inch thick FR4 board with SMA i/o ports. To minimize external losses, the dimensions of the board were kept smaller than a wavelength at the operating frequency. Power matching was achieved by adding external bond-wire inductors to the base and emitter of the input transistors; see Figure 1a and 1b. The values of external bond-wire inductors to the base and at the emitter of T1 were selected such that the input impedance to the amplifier was fairly close to 50 ohms. In order to improve the matching condition, additional SMD chip inductor was added in series with the inductive base bond-wires. In our simulations, we also included the parasitic effects associated with the pads.

#### Optimum Noise Matching

Noise matching was achieved by first determining the optimum noise impedance,  $Z_{opt}$ , of a single finger transistor biased at  $V_{CE}=1\text{V}$  and  $V_{BE}=0.81$ . To achieve noise matching,  $N$  number of fingers were added such that  $N=R_{opt}/(1/\mu_{eff}/50\Omega)$ . A value of  $N$ -fingers were used in our initial simulations, but was modified to take into account the external emitter and base bond wire inductance, and the various other components.

### Capacitively Coupled Resonator

The capacitively coupling elements in the low voltage circuit was optimized to enforce: (i) majority of the transconductance RF current generated by  $T1$  should be fed into  $T2$ , and (ii) to prevent oscillations the gain at the collector of  $T1$  was near unity.

### Layout

For comparison, we have ensured that optimal power and noise matching was achieved for both designs. Furthermore, we have ensured that both designs have similar layouts (i.e. they are mirror images of each other) except for the use of the capacitively coupled resonating element in the low voltage topology. In addition, both bipolar transistors  $T1$  and  $T2$  on both designs were made geometrically identical.

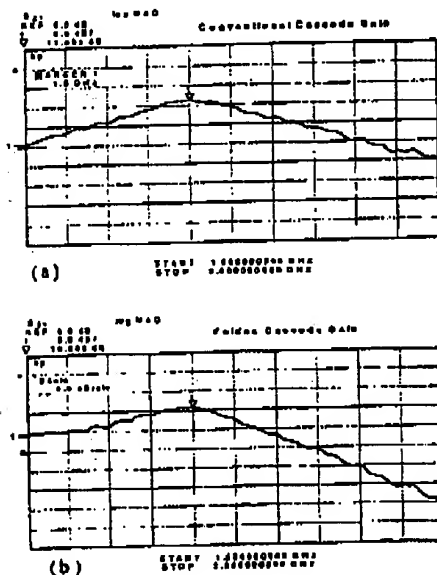


Figure 3: S21 dB: (a) Folded Cascode LNA and (b) Conventional Cascode LNA

### IV. Results and Conclusions

Figure 3 shows the measured gain (S21 dB) for both the folded and classic cascode structures. The characteristics are very similar. However, the folded structure has an additional 5dB gain at the lower band edge at 1.5 GHz and tends to have a faster roll off on the upper band edge at 2.5GHz. The losses associated in the external LC matching circuit have contributed to the reduced gain.

The distortion characteristics were measured using two tones at 1.885GHz and 1.905 GHz. The measured IIP3 and 1-dB compression points for both designs are shown in Figure 4. The folded cascode LNA has better linearity than

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the conventional cascode. The 1V structure had an IIP3 of -3.7 dBm, whereas the conventional cascode operating at 2V has an IIP3 of -7.9dBm. The enhancement in IIP3 is due to the phase and filtering response of the LC tanks.

The variation of IIP3 with the DC supply voltage is shown in Figure 5. The supply voltage of the folded cascode was brought down to 0.8V whereas for the conventional cascode it was brought down to 1.5V. The IIP3 of the folded cascode has a maximum value of 0dBm for a supply voltage of 1.5V (i.e. 6mW of DC power). The conventional cascode was measured to have an IIP3 of -14dBm at 1.5V (i.e. 3mW of DC power). This 3mW increase in power for the folded cascode is only a minor power penalty considering the 14dB increase in IIP3.

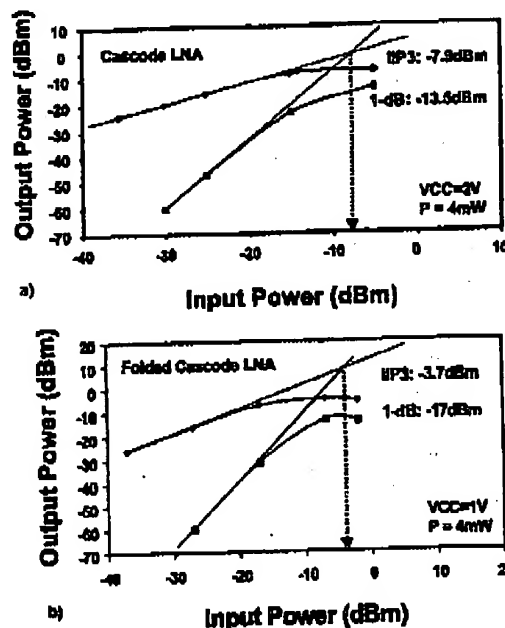


Figure 4: Distortion Characteristics: (a) conventional cascode LNA at 2V (b) folded cascode LNA at 1V.

Figure 6 summarizes the test results for both amplifiers. The noise figures of the folded and classical cascode were measured to be 2.3dB and 2.1dB, respectively when matched for maximum power.

When matched for noise, the minimum noise figure was measured to be 2.0 dB and 1.9dB for the folded and classic cascode structures respectively. Since the measured value of the minimum noise figure was close to the noise figure when the devices were power matched, implies that both structures were matched for noise and power.

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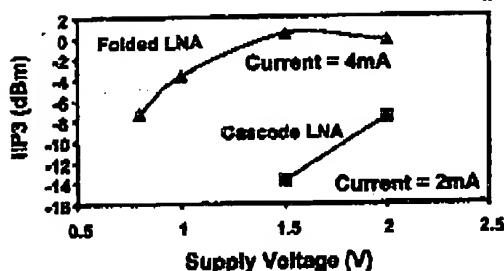


Figure 5: IIP3 as a function of supply voltage for the folded and conventional cascode LNA's.

Figure 6 also compares our results to other low voltage LNA's found in the literature

The 1V classical cascode by Callaway had a relatively low IIP3 of -22dB. The low voltage topology by Long *et al.* was implemented within a SiGe bipolar process and was measured to having an IIP3 of -4.5dB and a noise figure at 50Ω of 1.75dB. However, the minimum noise figure was determined to be 0.95dB.

These low noise figure values are a strong function of the SiGe-base structure. The results of a CMOS 1.5GHz LNA are also summarized in Figure 6. For this structure, a significant amount of power was required in order to reduce the noise figure to 3.5dB.

#### V. References

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- [3] Derek K. Shaeffer and Thomas H. Lee "A 1.5V 1.5GHz CMOS Low Noise Amplifier," IEEE J. Solid State Circuits, vol. 32, pp. 745-759, 1997.
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| Parameters | Folded (This work) | Cascode (This Work) | Cascode [2], Callaway | Transformer coupled [3] Long et al. | CMOS Cascode [4] (Shaeffer) |
|------------|--------------------|---------------------|-----------------------|-------------------------------------|-----------------------------|
| Technology | Si BJT             | Si BJT              | Si BJT                | SiGe HBT                            | CMOS 0.5μm                  |
| DC SUPPLY  | 1V                 | 2V                  | 1V                    | 1V                                  | 1.5V                        |
| Frequency  | 1.9 GHz            | 1.9 GHz             | 930 MHz               | 2.4 GHz                             | 1.5 GHz                     |
| POWER      | 40mW               | 4.0mW               | 1.1mW                 | 2.5mW                               | 30mW                        |
| GAIN       | 18.9 dB            | 11.8dB              | 15.0dB                | 11.0dB                              | 22.0dB                      |
| IIP3m      | -3.7 dBm           | -7.9 dBm            | -22 dBm               | -4.5 dBm                            | -9.5 dBm                    |
| 1-dBm      | -17 dBm            | -13.5 dBm           |                       |                                     | -22 dBm                     |
| NF(50Ω)    | 2.3 dB             | 2.1 dB              | 2.0 dB                | 1.75 dB                             | 3.5 dB                      |
| NFmin      | 2.0 dB             | 1.9 dB              |                       | 0.95 dB                             |                             |
| S11        | -17 dB             | -13 dB              |                       |                                     | -14 dB                      |
| S22        | -16 dB             | -15 dB              |                       |                                     |                             |

Figure 6: Performance summary and comparison between other low noise low voltage LNA's.